REMARKS

Claims 1-10 remain pending in this application for which applicant seeks reconsideration.

Amendment

Claims 1-10 have been cancelled and new claims 11-23 have been added.

Art Rejection

Claims 1-10 were rejected under 35 U.S.C. § 102(b) as anticipated by Yajima (USP 5,809,176). Applicant respectfully submits that the new claims clearly define over Yajima within the meaning of § 102 and § 103.

According to the present invention as claimed in claim 11, there is provided an arithmetic decoding method of decoding arithmetically encoded image data formed of at least one bitplane, by using a single arithmetic operation section and a plurality of memories that can be accessed separately. The method includes receiving information on a bit depth of the arithmetically encoded image data; storing, when the bit depth of the arithmetically encoded image data is equal to a number of the memories, state variables corresponding to pixels to be decoded, of respective bitplanes of the image data in respective corresponding ones of the memories; storing, when the bit depth of the arithmetically encoded image data is less than the number of the memories, one of the state variables corresponding to pixels to be decoded, of each bitplane of the image data, in at least part of the memories by allocating the one of the state variables thereto; reading ones of the state variables corresponding, respectively, to pixels to be decoded, of each bitplane, from the memories; selecting ones of the state variables read from the memories based on data which have been arithmetically encoded by the arithmetic operation section; and

inputting the selected ones of the state variables and values of a more probable symbol which are paired with the selected ones of the state variables, to the arithmetic operation section. The claimed method enables inexpensive processing of both of binary image data and multi-level image data.

Yajima relates generally to image data encoding and decoding devices and processes employing fast, efficient arithmetic coding techniques (col. 1, lines 8-11). Yajima aims to increase performance in image data encoder/decoder systems without having to increase clock speeds of the constituent elements (col. 3, lines 25-28). In Yajima, an arithmetic decoder system 4 has four arithmetic decoders corresponding to four encoders of an arithmetic encoder system 2. The arithmetic decoder system 4 comprises four memory means 18-1 to 18-4, input interfaces 20-1 to 20-4, and arithmetic decoders 22-1 to 22-4 (col. 11, lines 55-62). The arithmetic decoders 22-1 to 22-4 decode, respectively, incoming encoded data streams 200-1 to 200-4 following the exactly reversed procedures of those for corresponding arithmetic encoders 10-1 to 10-4 and output to a data multiplexer 34 resultant image data streams 110-1 to 110-4, each of which forms a bit plane of the image (col. 12, lines 9-15). Since the arithmetic decoder system 4 decodes four encoded data streams in parallel, it can generate image data four times as fast as the conventional system compared to conventional decoders operating on the same type of image data (col. 12, lines 28-32).

Yajima, however, merely discloses decoding, respectively, a plurality of encoded data streams using known arithmetic decoders arranged in parallel. Yajima dicloses dividing image data into a plurality of bitplanes before being input to the arithmetic decoders (col. 11, line 54 to cl. 12, line 58). However, Yajima does not disclose nor suggest receiving information on the bit depth of the encoded image data, and does not disclose or suggest switching the storage method

of storing state variables in memory means, according to the information on the bit depth.

Namely, the construction of Yajima is based on the assumption that the number of bits of the encoded data and the number of the arithmetic decoders are always the same. As is distinct from this, the present invention aims to realize arithmetic decoding of plural types of image data having different numbers of bits using an inexpensive construction, and is characterized by providing control to switch the storage method of storing state variables in memory means and carry out decoding using a single arithmetic operation section and a plurality of memories, according to the information on the bit depth of the image data to be decoded.

Accordingly, none of the above described features of the claimed present invention is taught or suggested by Yajima

Conclusion

Applicant submits that the pending claims patentably distinguish over the applied references and are in condition for allowance. Should the examiner have any issues concerning this reply or any other outstanding issues remaining in this application, applicant urges the examiner to contact the undersigned to expedite prosecution.

Respectfully submitted,

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